REMARKS

Claims 1-12 are presently pending and stand rejected. Reconsideration is requested.

Claims 1-12 were rejected under 35 U.S.C. 102(b) as being anticipated by Rana. To anticipate a claim, the reference must teach every element of the claim. MPEP 2131. Claims 1 and 9 recite, among other limitations, "the contents of the memory location associated with the address received from the code address bus being incremented responsive to receipt of the address". Claim 5 recites, among other limitations "incrementing a memory location mapped to the address associated with the instruction".

Examiner has indicated that "Rana also teaches the code coverage memory storing code coverage data of predetermined bit patterns that includes hexadecimal value '00' and changed to value 'ff', this is interpreted as the contents of the memory location associated with the address received from the code address bus being incremented responsive to the receipt of the address."

Rana, Col. 8, Lines 31-44 states that "For example, hexadecimal 'ff' may be loaded from the register 58 to the code coverage memory 10 in one test, and hexadecimal '00' may be loaded in another test." (Emphasis Added). Assignee submits Rana does not teach that "hexadecimal value '00'" is "changed to value 'ff'" as indicated by Examiner. Rather, "hexadecimal 'ff' may be loaded from the register 58 to the code coverage memory 10 in one test, and hexadecimal '00' may be loaded in another test." Moreover it is also submitted that even if "hexadecimal value '00'" is "changed to value 'ff'", the foregoing does not amount to incrementing.

Accordingly, Assignee traverses the rejection to claims 1, 5, and 9, and dependent claims 2-4, 6-8, and 10-12, because Rana does not teach that "the contents of the memory location associated with the address received from the code address being incremented responsive to the receipt of the address".

Claim 2 recites, among other limitations, "an address multiplexer for making a selection between the input and an address counter, and for providing the selection to the memory".

Examiner has indicated that Rana discloses 'the code coverage memory being concurrently addressed with the monitored memory and the use of a counter circuit of memory location, this is interpreted as an address multiplexer for making a selection between the input and an address counter, and for providing the selection to the memory (See Col. 4, line 65 to Col. 5, line 3 and Col. 5, lines 11-18)."

"Claims must be given their broadest reasonable interpretation." MPEP 2111. However, the broadest reasonable interpretation of "an address multiplexer for making a selection between the input and an address counter" cannot be interpreted to cover merely "code coverage memory being concurrently addressed with the monitored memory and the use of a counter circuit of memory location", even if the foregoing characterization is correct. It is noted that the foregoing does not teach a "multiplexer" or selecting "between the input and an address counter". Accordingly, Assignee traverses the rejection to claim 2 and requests that Examiner withdraw the rejection.

Claim 3 recites "a data multiplexer for making a selection between an increment signal and a clear signal, and for providing the selection to the memory". Examiner has indicated that "Rana teaches the code coverage memory storing code coverage data of predetermined bit patterns that includes setting the hexadecimal value to '00' and changing it to value 'ff', this is interpreted as a data multiplexer for making a selection between an increment signal and a clear signal, and for providing the selection to the memory (See Col. 8, lines 31-44)."

Rana, Col. 8, Lines 31-44 states that "For example, hexadecimal 'ff' may be loaded from the register 58 to the code coverage memory 10 in one test, and hexadecimal '00' may be loaded in another test." (Emphasis Added). Assignee submits Rana does not teach that "hexadecimal value '00'" is "changed to value 'ff'" as indicated by Examiner. Rather, "hexadecimal 'ff' may be loaded from the register 58 to the code coverage memory 10 in one test, and hexadecimal '00' may be loaded in another test." Moreover it is also submitted that even if "hexadecimal value '00'" is "changed to value 'ff'", the foregoing does not amount to incrementing. Accordingly, Assignee traverses Examiner's characterization of Rana.

Moreover, the broadest reasonable interpretation of "a data multiplexer for making a selection between an increment signal and a clear signal, and for providing the selection to the memory" cannot be interpreted to cover merely "the code coverage memory storing code coverage data of predetermined bit patterns that includes setting the hexadecimal value to '00' and changing it to value 'ff'", even if the foregoing characterization of Rana is correct. It is noted that the foregoing does not explicitly teach a

"multiplexer", or selecting "between an increment signal and a clear signal". Accordingly, Assignee traverses the rejection to claim 3 and requests that Examiner withdraw the rejection.

Claim 10 recites, among other limitations, "an address multiplexer connected to the input and address counter, the address multiplexer making a selection between the input and an address counter, and for providing the selection to the memory".

Examiner has indicated that Rana discloses "the code coverage memory being concurrently addressed with the monitored memory and the use of a counter circuit of memory location, this is interpreted as an address multiplexer connected to the input and address counter, the address multiplexer making a selection between the input and an address counter, and for providing the selection to the memory (See Col. 4, line 65 to Col. 5, line 3 and Col. 5, lines 11-18)."

Assignee submits that the broadest reasonable interpretation of "an address multiplexer connected to the input and address counter, said address multiplexer for making a selection between the input and an address counter, and for providing the selection to the memory" cannot be interpreted to cover merely "code coverage memory being concurrently addressed with the monitored memory and the use of a counter circuit of memory location", even if the foregoing characterization is correct. It is noted that the foregoing does not teach a "multiplexer", selecting "between the input and an address counter", or "providing the selection to the memory". Accordingly, Assignee

traverses the rejection to claim 10 and requests that Examiner withdraw the rejection.

Claim 11 recites "a data multiplexer connected to the memory, the data multiplexer selecting between an increment signal and a clear signal, and providing the selection to the memory". Examiner has indicated that "Rana teaches the code coverage memory storing code coverage data of predetermined bit patterns that includes setting the hexadecimal value to '00' and changing it to value 'ff', this is interpreted as a data multiplexer connected to the memory, the data multiplexer selecting between an increment signal and a clear signal, and for providing the selection to the memory (See Col. 8, lines 31-44)."

Rana, Col. 8, Lines 31-44 states that "For example, hexadecimal 'ff' may be loaded from the register 58 to the code coverage memory 10 in one test, and hexadecimal '00' may be loaded in another test." (Emphasis Added). Assignee submits Rana does not teach that "hexadecimal value '00'" is "changed to value 'ff'" as indicated by Examiner. Rather, "hexadecimal 'ff' may be loaded from the register 58 to the code coverage memory 10 in one test, and hexadecimal '00' may be loaded in another test." Moreover it is also submitted that even if "hexadecimal value '00'" is "changed to value 'ff'", the foregoing does not amount to incrementing. Accordingly, Assignee traverses Examiner's characterization of Rana.

Moreover, the broadest reasonable interpretation of "a data multiplexer connected to the memory, the data multiplexer selecting between an increment signal and a clear signal, and providing the selection to the memory" cannot be interpreted to cover merely "the code coverage memory storing code coverage data of predetermined bit

patterns that includes setting the hexadecimal value to '00' and changing it to value 'ff'", even if the foregoing characterization of Rana is correct. It is noted that the foregoing does not explicitly teach a "multiplexer", or selecting "between an increment signal and a clear signal". Accordingly, Assignee traverses the rejection to claim 11 and requests that Examiner withdraw the rejection.

Claim 13 is added, and recites, among other limitations, "wherein the contents of the memory location associated with the address received from the code address bus are incremented responsive to receipt of the address, thereby indicating a number of times the address has been received" (Emphasis Added).

Allowance for claim 13 is requested, on the basis that claim 13 is dependent on claim 1 which is allowable, as well as because Rana does not teach the foregoing limitation. Even if Rana was characterized as teaching that "the code coverage memory storing code coverage data of predetermined bit patterns that includes hexadecimal value '00' and changed to value 'ff'", Rana does not teach "wherein the contents of the memory location associated with the address received from the code address bus are incremented responsive to receipt of the address, thereby indicating a number of times the address has been received". It is submitted that "hexadecimal value '00'" "changed to 'ff'" does not teach "indicating a number of times the address has been received."

Accordingly, allowance is respectfully requested for claim 13.

CONCLUSION

For at least the foregoing reasons, Assignee submits that each of the pending claims are now in a condition for allowance. Accordingly, Examiner is requested to pass this case to issuance.

It is believed that all monies for the actions described herein are provided with this correspondence. To the extent that additional monies are required for any of the actions requested in the correspondence, Commissioner is authorized to charge such fees and credit any overpayments to deposit account 13-0017.

Respectfully Submitted

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